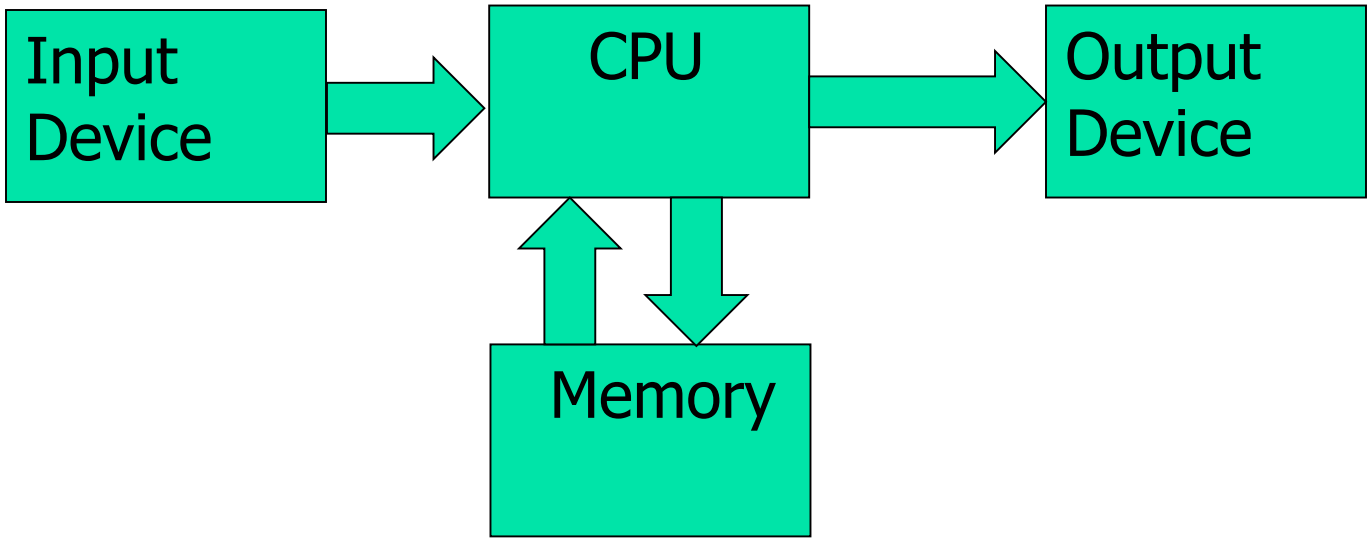
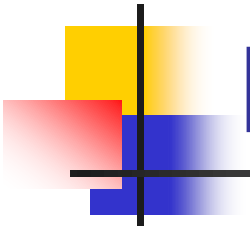
Architecture of 8085

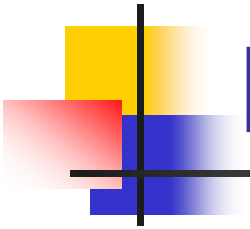
Block Diagram Computer





Processor System Architecture

- Input Devices
- Output Devices
- Memory
- CPU
- Busses
  - Address Bus
  - Data Bus
  - Control Bus

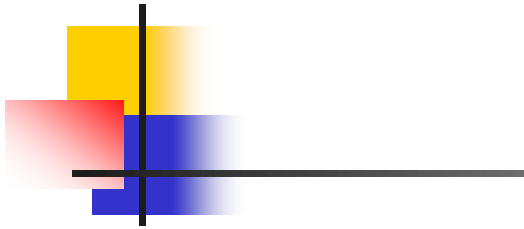


Busses

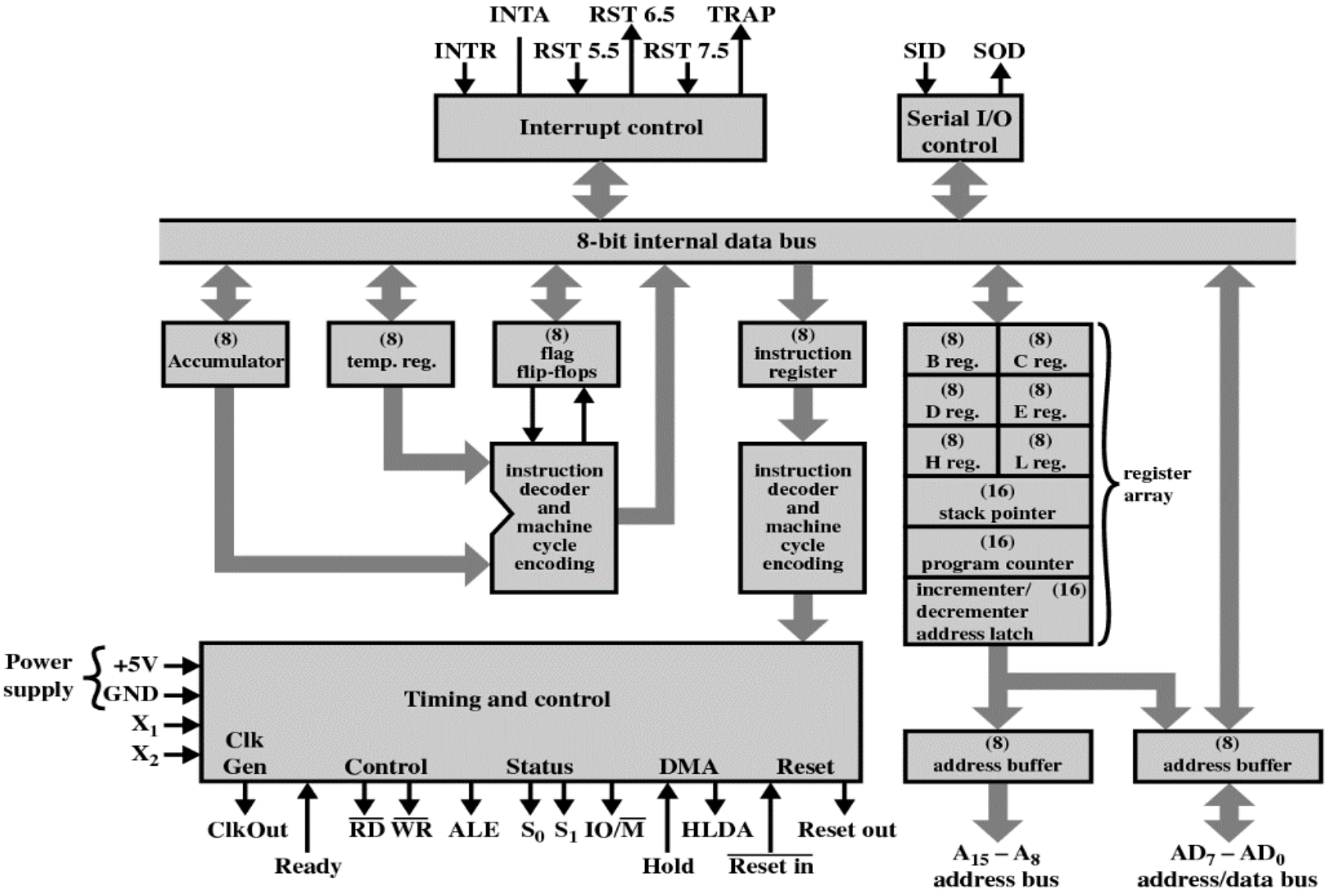
- A group of wires used to communicate signals among devices
  - Address bus for address (Unidirectional)
  - Data bus for data exchange (Bidirectional)
  - Control bus for control signals

Features of 8085

- 8 bit microprocessor
- HMOS technology
- 80 instructions
- 246 opcodes
- 3 MHz
- 5 V power supply



The 8085 Microprocessor Architecture


INTA
RST 6.5
TRAP
INTR
RST 5.5
RST 7.5
SID
SOD
Interrupt control
Serial I/O control
8-bit internal data bus
(8) Accumulator
(8) temp. reg.
(8) flag flip-flops
(8) instruction register
(8) B reg.
(8) C reg.
(8) D reg.
(8) E reg.
(8) H reg.
(8) L reg.
(16) stack pointer
(16) program counter
incrementer/ decrementer address latch
(16)
register array
instruction decoder and machine cycle encoding
instruction decoder and machine cycle encoding
Power supply
+5V
GND
X1
X2
Timing and control
Clk Gen
Control
Status
DMA
Reset
ClkOut
Ready
RD
WR
ALE
S0
S1
IO/M
Hold
HLDA
Reset in
Reset out
(8) address buffer
(8) address buffer
A15 – A8 address bus
AD7 – AD0 address/data bus

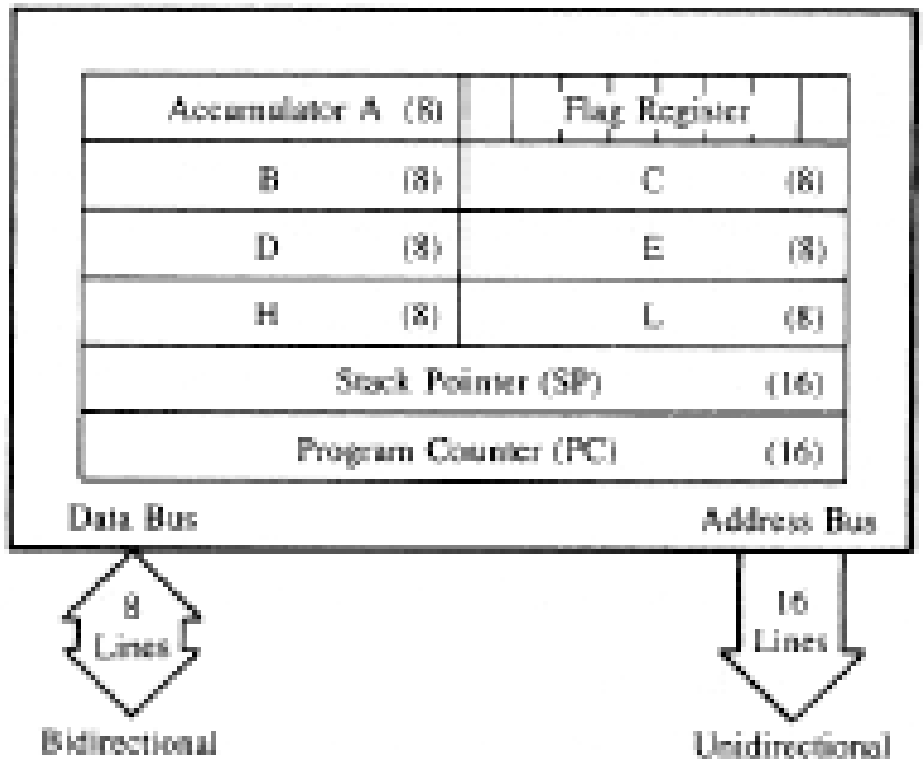
Architecture of 8085

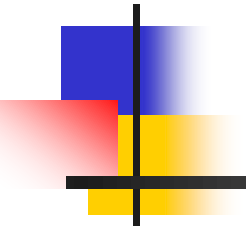
- 8085 architecture consists of following blocks:
  - ALU logic
  - Register Logic
  - Timing and Execution Logic
  - Interrupt Logic
  - Serial I/O Logic

The ALU

- Performs Arithmetic and Logical operations
- In addition to the arithmetic & logic circuits, the ALU includes the accumulator, which is part of every arithmetic & logic operation.
- Also, the ALU includes a temporary register used for holding data temporarily during the execution of the operation. This temporary register is not accessible by the programmer.

Registers of 8085





Register Section

- General Purpose Registers
  - A, B, C, D, E, H, and L
  - BC, DE, and HL
- Special Function Registers
  - Program Counter
  - Stack Pointer

Program counter

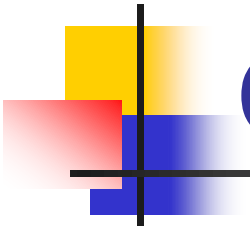
- Keeps track of what instruction is being used and what the next instruction will be.
- 16 bit long.
- Can get data from internal bus as well as memory location.
- Automatically increments to point to the next memory during the execution of the present instruction.
- PC value can be changed by some instructions.

Stack pointer

- 16 bit register acts as memory pointer.
- Can save the value of the program counter for later use.
- Points to a region of memory which is called stack. follows LIFO algorithm.
- After every stack operation SP points to next available location of the stack. Decrements in 8085.

Memory address register

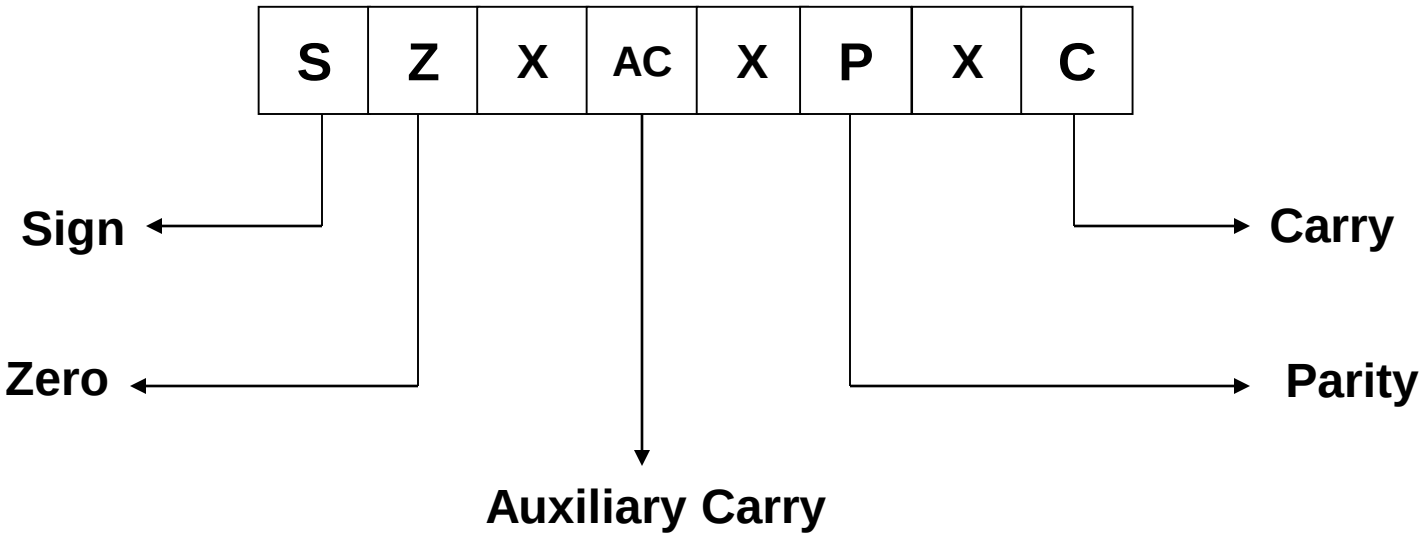
- PC sends address to MAR. MAR points to the location of the memory where the content is to be fetched from.
- PC increments but MAR does not.
- If the content is an instruction, IR decodes it. During execution if it is required to fetch another word from memory, PC is loaded with the value
- PC again sends it to the MAR and fetch operation starts.



Others

- Instruction decoder.
- Control logic.
- Internal data bus.

Flag register



X - Unspecified

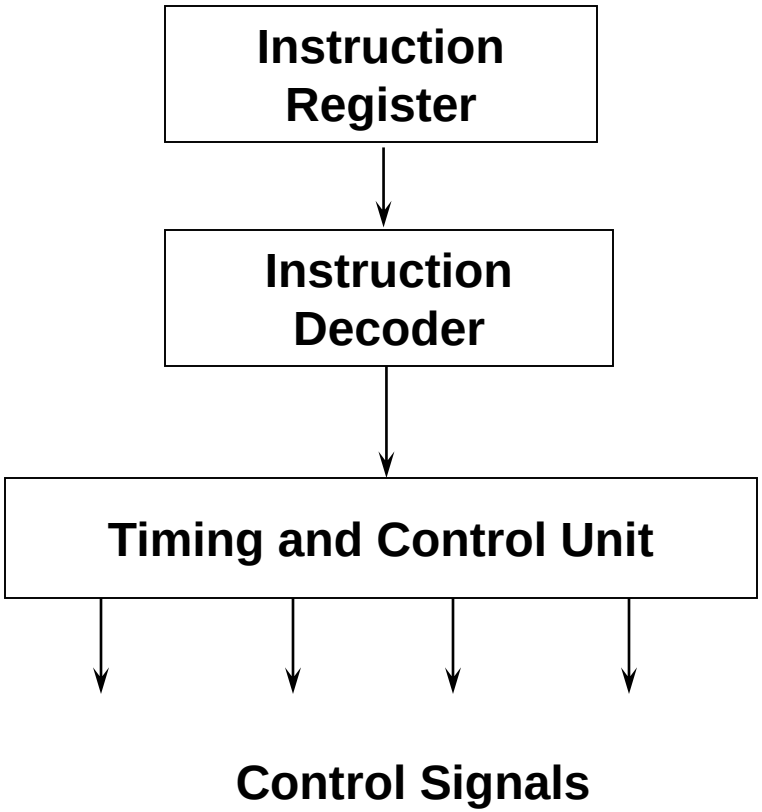
The Flags register

- There is also the flags register whose bits are affected by the arithmetic & logic operations.
  - S-sign flag
    - The sign flag is set if bit D7 of the accumulator is set after an arithmetic or logic operation.
  - Z-zero flag
    - Set if the result of the ALU operation is 0. Otherwise is reset. This flag is affected by operations on the accumulator as well as other registers. (DCR B).

The Flags register

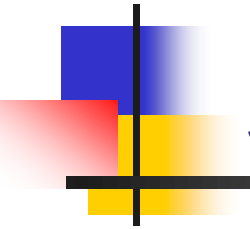
- AC-Auxiliary Carry
  - This flag is set when a carry is generated from bit D3 and passed to D4 . This flag is used only internally for BCD operations. (Section 10.5 describes BCD addition including the DAA instruction).
- P-Parity flag
  - After an ALU operation if the result has an even # of 1's the p-flag is set. Otherwise it is cleared. So, the flag can be used to indicate even parity.
- CY-carry flag
  - Discussed earlier

Timing and Execution Logic



Interrupt Logic

- Consists of 5 interrupts with following properties:
  - Priority
  - Maskable and Non Maskable
  - Vectored and Non – Vectored
- $\overline{\text{INTA}}$ is an output signal



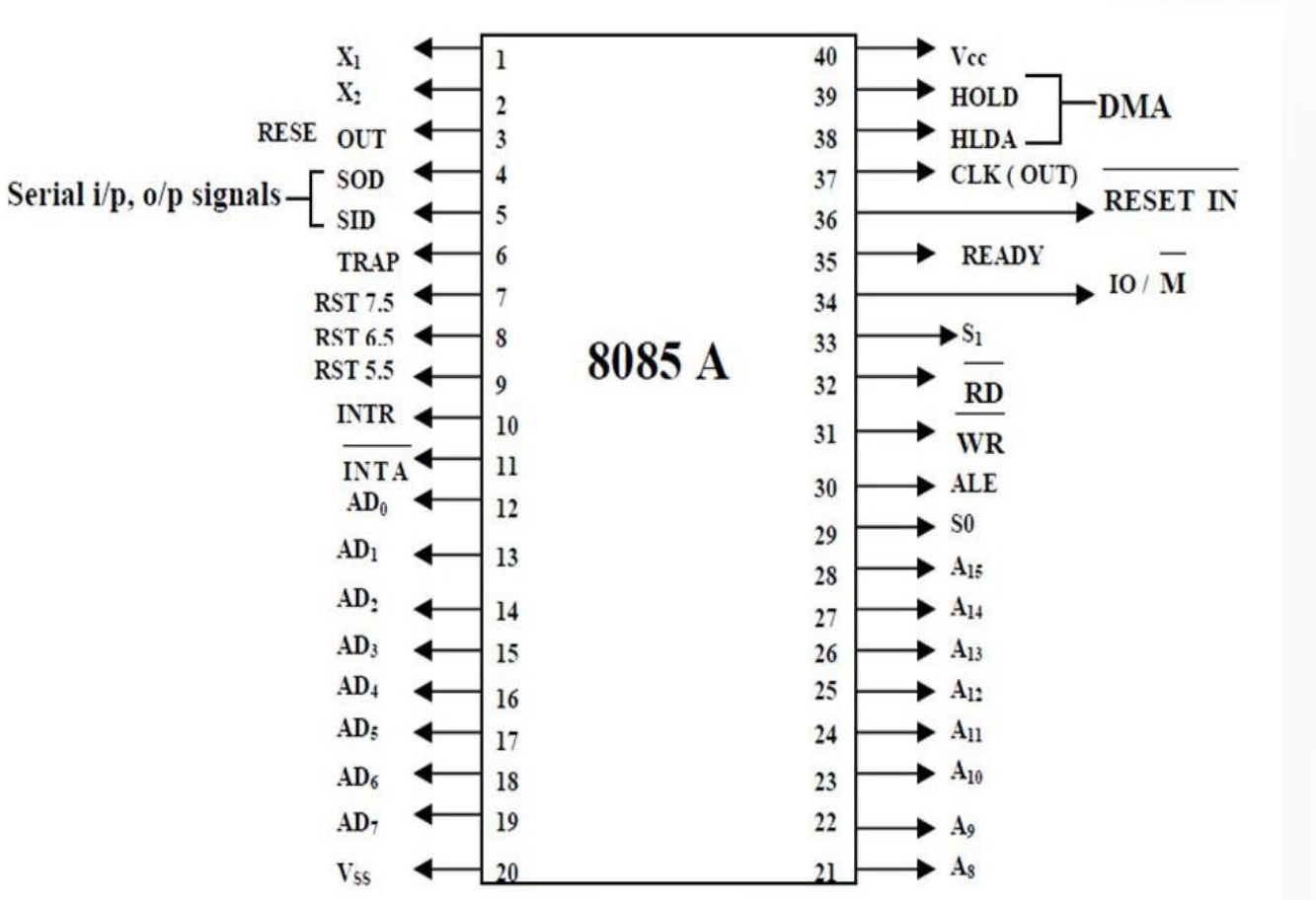
Serial I/O Logic

- Supports serial I/O using 2 lines
  - SID – Serial Input Data
  - SOD – Serial Output Data

The 8085 and Its Busses

- The 8085 is an 8-bit general purpose microprocessor that can address 64K Byte of memory.
- It has 40 pins and uses +5V for power. It can run at a maximum frequency of 3 MHz.
  - The pins on the chip can be grouped into 6 groups:
    - Address Bus.
    - Data Bus.
    - Control and Status Signals.
    - Power supply and frequency.
    - Externally Initiated Signals.
    - Serial I/O ports.

8085 pin diagram



The Address and Data Busses

- The address bus has 8 signal lines A8 – A15 which are unidirectional.
- The other 8 address bits are multiplexed (time shared) with the 8 data bits.
  - So, the bits AD0 – AD7 are bi-directional and serve as A0 – A7 and D0 – D7 at the same time.
    - During the execution of the instruction, these lines carry the address bits during the early part, then during the late parts of the execution, they carry the 8 data bits.

Frequency Control Signals

- There are 3 important pins in the frequency control group.
  - X0 and X1 are the inputs from the crystal or clock generating circuit.
    - The frequency is internally divided by 2.
      - So, to run the microprocessor at 3 MHz, a clock running at 6 MHz should be connected to the X0 and X1 pins.
  - CLK (OUT): An output clock pin to drive the clock of the rest of the system.
- We will discuss the rest of the control signals as we get to them.

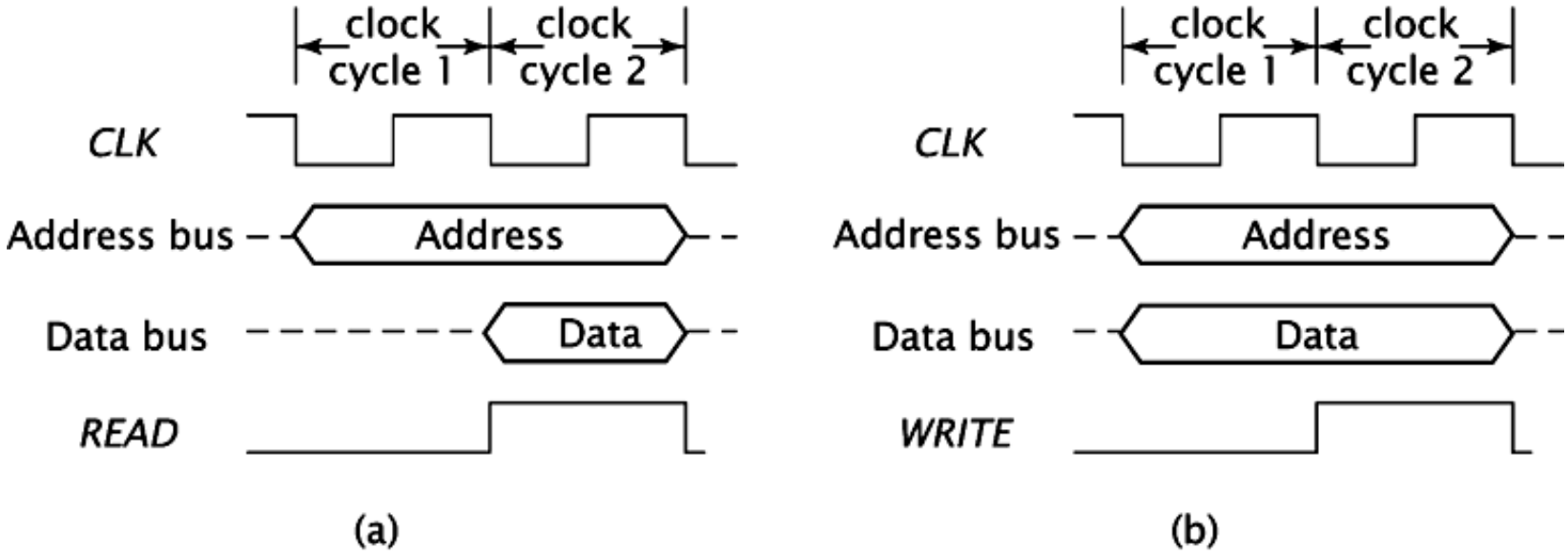
Instruction Cycle

- Instruction Cycle
  - the procedure a microprocessor goes through to process an instruction
- Fetch
  - Read instruction from memory
- Decodes
  - Determine which instruction it has fetched
- Execute
  - Perform necessary operations to execute the instruction

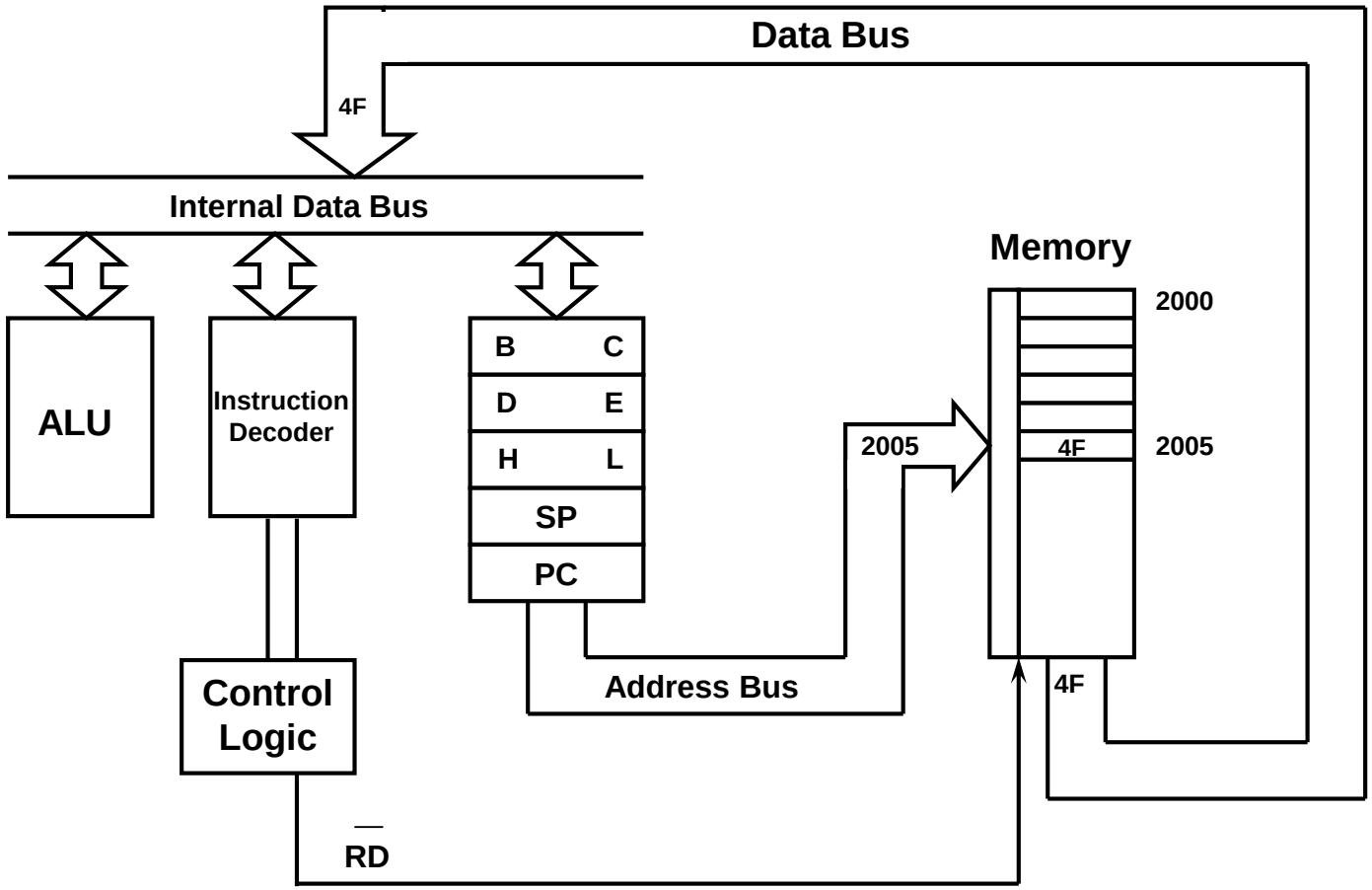
Instruction Cycle

- Read
  - A signal on the control bus which the microprocessor asserts when it is ready to read data form memory or an I/O device.
- Write
  - A signal that triggers memory to store data.

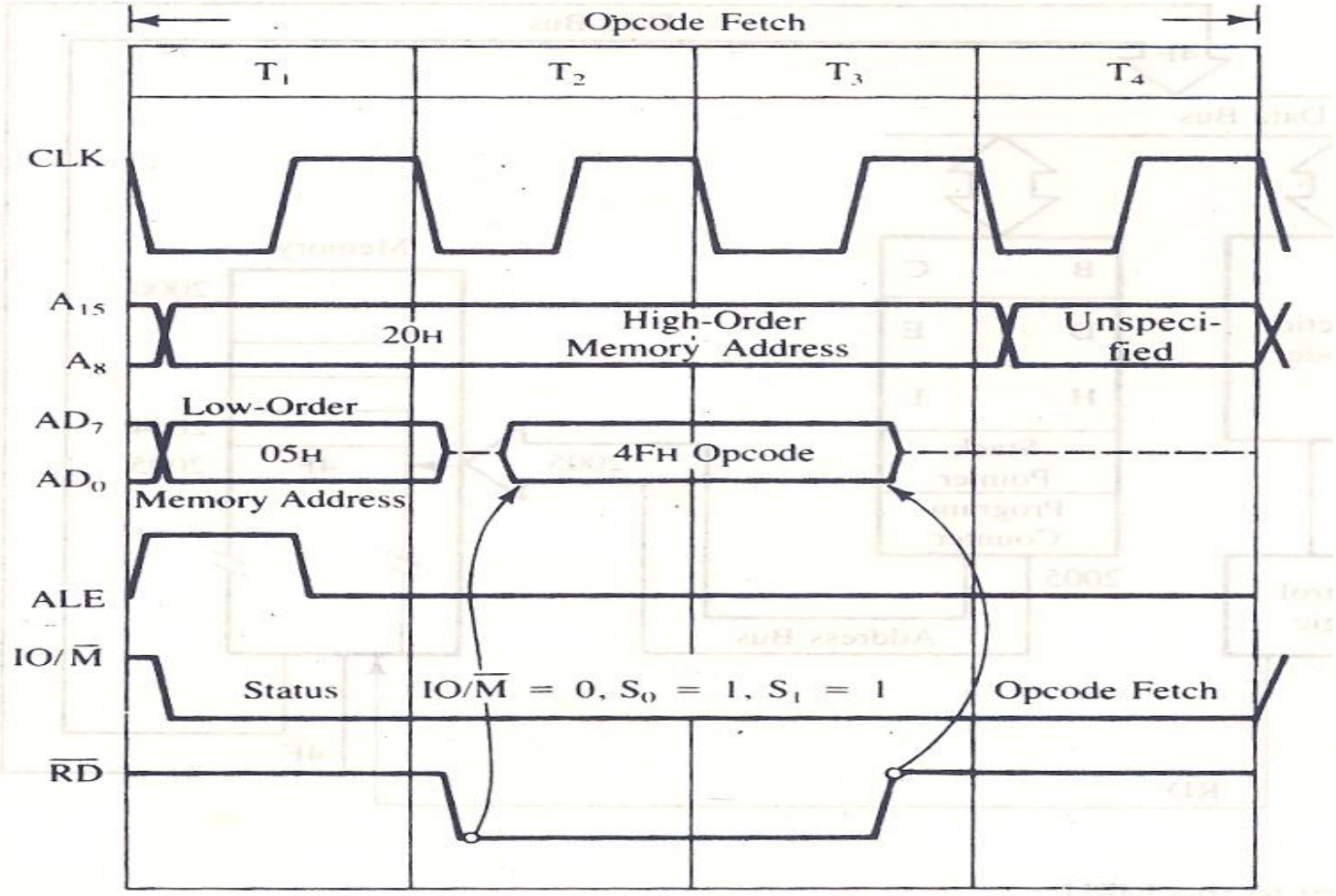
Timing diagram for (a) memory read (b) memory write operations



Mp Communication And Bus Timings

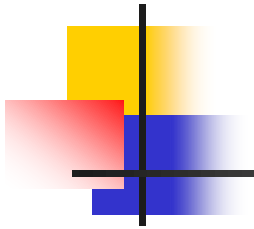


Timing Diagram



Cycles and States

- From the above discussion, we can define terms that will become handy later on:
  - T- State: One subdivision of an operation. A T-state lasts for one clock period.
    - An instruction's execution length is usually measured in a number of T-states. (clock cycles).
  - Machine Cycle: The time required to complete one operation of accessing memory, I/O, or acknowledging an external request.
    - This cycle may consist of 3 to 6 T-states.
  - Instruction Cycle: The time required to complete the execution of an instruction.
    - In the 8085, an instruction cycle may consist of 1 to 6 machine cycles.



Thanks